REMARKS

Present Status of the Application

It is noted with great appreciation that the Examiner indicated that Claim 15 is allowable over the prior art of record if rewritten in independent form including all of the limitations of the base Claim and any intervening Claims. Claims 10-16 are pending of which Claims 10 and 14-16 have been amended, Claims 11-13 have been canceled and Claims 17-19 have been added to more explicitly describe the claimed invention. More specifically, the subject matter of Claims 11, 12 and 13 have been incorporated into Claim 10. It is believed that no new matter adds by way of amendments made to Claims or otherwise to the application. For at least the foregoing reason, Applicant respectfully submits that Claims 10 and 14-19 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion of the Claim rejection under 35 USC 103

The Office Action rejected Claims 10-14 and 16 under 35 USC 103(a) as being unpatentable by Jung Lin et al. (US-6,087,222, hereinafter Jung Lin) in view of Lee et al. (US-5,773,343, hereinafter Lee).

Applicant respectfully disagrees and traverses the above rejections as follows. Independent Claim 10, as amended, is allowable for at least the reason that Jung Lin and Lee substantially fail to teach, suggest or disclose every features of the claimed invention. More specifically, both Jung Lin and Lee substantially fail to teach, suggest or disclose at least ***"a dielectric layer formed between the select gate and the substrate, wherein a portion of the dielectric layer is physically in contact with a sidewall of the trench and the select gate, as required by the amended Claim 10"***. The advantage of the above structure is that at least a lower voltage is required for turning on the select gate.

Instead, Jung Lin, in FIG. 1L and 4, substantially teaches a vertical transistor memory device including forming a floating gate FG in the trench and a control gate CG over the floating gate, a interelectrode dielectric 30 composed of ONO disposed in between the floating gate FG and the control gate CG and a tunnel oxide 22 disposed between the interelectrode dielectric 30 and the substrate 11 [within the trench]. In other words, the tunnel oxide 22 and an inter-electrode dielectric 30 comprised of ONO are disposed between the control gate CG and the substrate 11. Whereas, the amended Claim 10 specifies that a portion of the tunnel oxide is physically in contact with a portion of the sidewall of the trench and the select gate CG, i. e. only a tunnel oxide is

disposed in between the select gate CG and the substrate. Accordingly, Jung Lin cannot possibly meet the claimed invention in this regard.

Further, because the tunnel oxide 22 and an inter-electrode dielectric 30 comprised of ONO are disposed between the control gate CG and the substrate 11 within the trench, and therefore comparatively a higher voltage is required for turning on the control gate. In other words, because only a gate oxide is positioned between select gate and the substrate, and therefore a lower voltage is needed for turning on the select gate compared to that required by the control gate CG of Jung Lin. Therefore Jung Lin cannot possibly Claim 10 in this regard.

Further, like Jung Lin, Lee also, in FIG. 5, substantially shows that a tunnel oxide 47 and a dielectric layer 52 are disposed between the gate 53 and the substrate 41 within the trench 41 (46). In other words, Lee also substantially fails to teach, suggest or disclose a portion of the tunnel oxide in physical contact with the select gate and the substrate [within the trench]. Accordingly, Lee cannot meet the claimed invention in this regard.

Further, Lee fails to teach, suggest or disclose a structure of a split gate cell, instead, Lee teaches a structure of a semiconductor device having a recessed channel structure, wherein (please see FIG. 5) the (first) gate 53 over the floating gate 29, wherein the gate 53 is formed over the substrate 41, and because the gate 53 is separated from the substrate 41 by a thick oxide layer 43, and therefore the gate 53 of Lee does not function for controlling the tunnel under the tunnel oxide 47. Therefore, it is clear that the semiconductor device of Lee is not a split gate cell.

For at least the above reasons, Applicant respectfully submits that no combination of Jung Lin and Lee can possibly render every features of Claims 10 and 14-19 of the claimed invention obvious and therefore Claims 10 and 14-19 should be allowed. Reconsideration and withdrawal of these rejections is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending Claims 10 and 14-19 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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